

Replace the paragraph beginning at line 4 on page 9 with the following:

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Fig. 2 illustrates trenches 16 having been filled with an insulating dielectric material 20, such as high density plasma deposited oxide, and subjected to a planarization step to provide a substantially planar outer surface. At this point in the process, such effectively forms an alternating series of trench isolation regions 22 and active area regions 18 in semiconductor substrate 11 running in a line adjacent and along lines of floating gates 12 and 14. The semiconductor wafer is typically and preferably fabricated to a point as would be depicted in Fig. 2, with the lines of floating gates being fabricated thereafter. Lines of floating gates 12 and 14 preferably constitute a gate dielectric layer (not shown), floating gate regions 23 (Fig. 1), an interpoly dielectric layer (not shown), a conductively doped polysilicon/silicide stack (not shown), and an insulative cap (not shown). (Such "not shown" items of this first described embodiments are shown in the embodiments of Figs. 7-9.)

Replace the paragraph beginning at line 22 on page 13 with the following:

Another implementation is described with reference to Figs. 6-7. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Fig. 6 is a sectional view or cut corresponding to that of Fig. 2, and depicts processing occurring subsequent to that of Fig. 2. Accordingly, an array 10b in accordance with this particular preferred embodiment is processed initially to the point as depicted in Fig. 2 in the first-described embodiment. A series of alternating trench isolation regions 22 and active areas 18 are thereby provided within semiconductor substrate 11 in a line adjacent and along at least a portion of lines of floating gates 12 and 14. Such defines a series of discrete transistor source areas separated by trench isolation regions. Floating gate word line patterning thereafter occurs, followed by drain region formation as described above. Lines of floating gates 12 and 14 as depicted in Fig. 7 (as well as in Figs. 8 and 9 described subsequently) comprise a gate dielectric layer, floating gate regions 23 formed thereover, an interpoly dielectric layer formed over floating gate regions 23, a conductively doped polysilicon/silicide stack formed over the interpoly dielectric layer, and an insulative cap (having an

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outermost surface) formed over the conductively doped polysilicon/silicide stack.

Replace the paragraph beginning at line 16 on page 15 with the following:

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The photoresist is subsequently stripped, and an electrically insulative spacer forming layer is deposited over the entirety of the wafer. Such is ideally comprised of a different material than gate dielectric layer 43 of lines 12 and 14. Circuitry peripheral to the array is then preferably masked such that the entirety of the array remains open. Spacers for the lines of floating gates within the array, such as the depicted spacers 42 in Fig. 7 and having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface, are then formed by anisotropic etching to electrically isolate the sides of the lines of floating gates. Such preferably does not occur yet in the periphery which is why it is masked, as the preferred subsequently deposited polysilicon would otherwise result in polysilicon on monocrystalline silicon in the preferred embodiment over the peripheral transistor and other circuitry active areas. Unetched material 43 over drain locations 24 will separate monocrystalline silicon from polysilicon in this example embodiment. Alternately, if the peripheral gates are also initially formed such that the bottom gate dielectric layer is not etched and comprises a material different from the spacer layer, this material will separate polysilicon from monocrystalline silicon such that masking of the spacer forming layer in the periphery is immaterial.